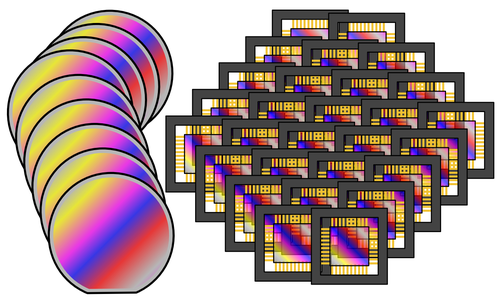
Computer Architectures for Chip Surplus

August Ning, David Wentzlaff

PRINCETON UNIVERSITY

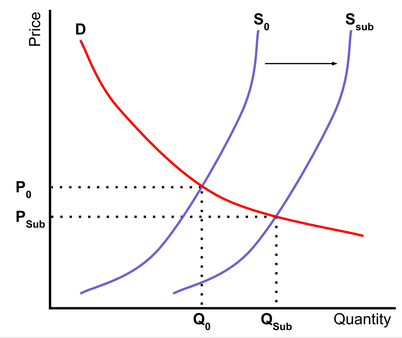
Chip Surplus

- Foundries are reluctant to reduce operations as die yield and productivity decrease during restarts
- Companies have hoarded chips and may decrease foundry orders when manufacturing capacity returns
- Decreased global semiconductor demand in the face of economic down turns hints at a future chip surplus



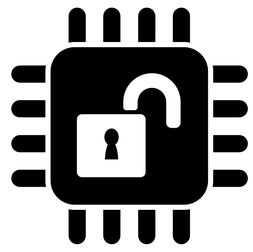
Semiconductor Subsidies

- Securing semiconductor supply has become a economic and national security priority
- Government subsidies for chip manufacturing and foundries' own investments will increase chip manufacturing supply in the future

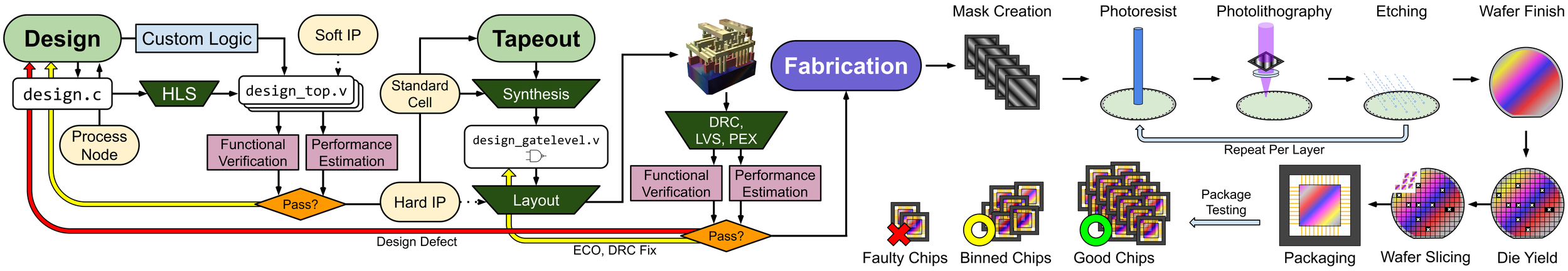


Cheaper Designs, Tools, and Tapeouts

- Open-sourced hardware designs, CAD tools, soft IP, and PDKs significantly lower the financial barriers to entry into designing and manufacturing chips
- Open-sourced frameworks allow architects to quickly generate designs, validate, and tapeout
- Reducing design and tapeout time reduces engineering salary costs



Chip Creation is Specialized, Time Consuming, and Expensive

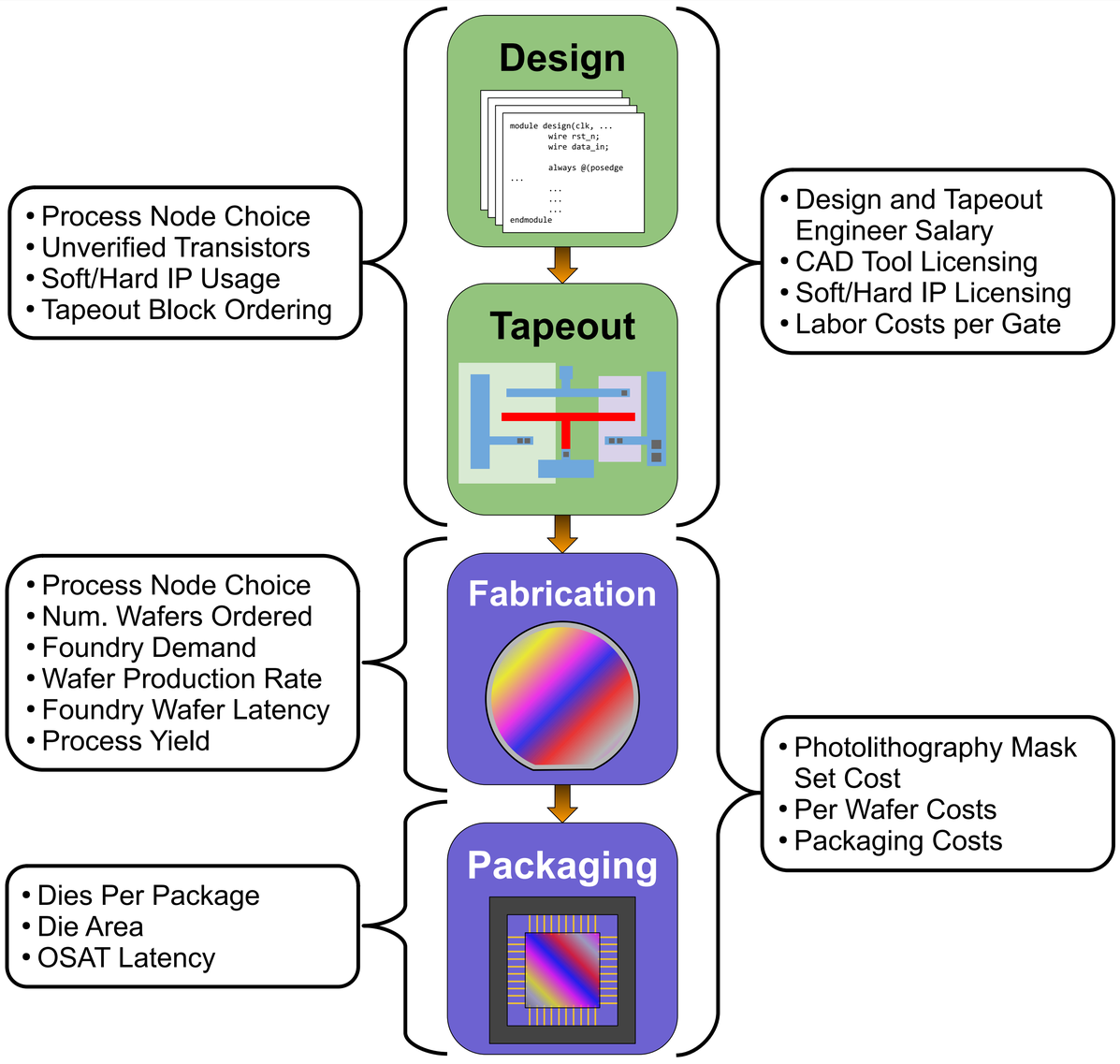


- Chip design requires expertise in chip architecture, backend tapeout flow, and verification
- Fabrication is a complex process and only few firms manufacture at the most advanced nodes
- Five semiconductor foundries control 90% of pure-play production capacity

- Chip designs take require multiple iteration to meet performance, cost, and area constraints
- Synthesis, layout, and verification take significant engineering effort and compute time
- A single wafer may take 12-20 weeks to complete fabrication and additional time to complete packaging

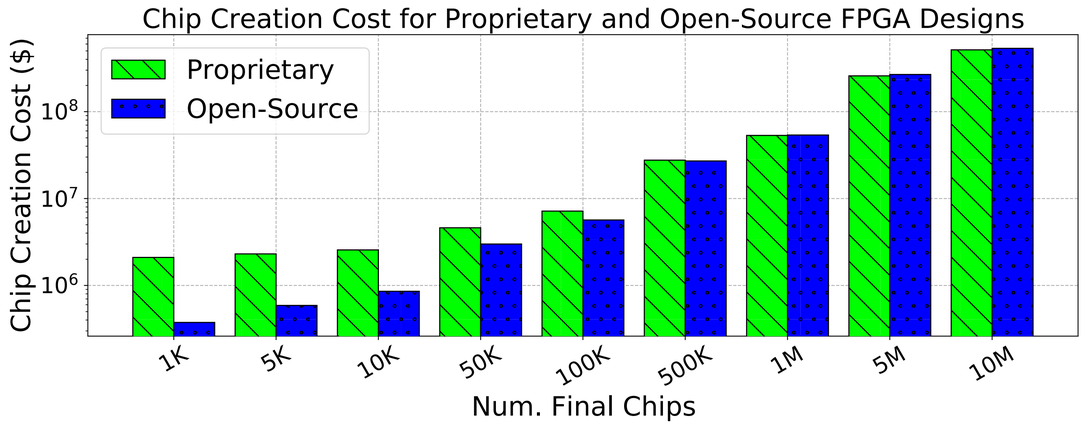
- Chip design CAD tools, IP, and PDKs generally require expensive licenses
- Specialization and expensive raw inputs means photolithography masks and wafer costs dominate
- Few competitors and market monopolies mean foundries have low pressure to reduce prices

Time-to-Market and Moonwalk Cost Modeling

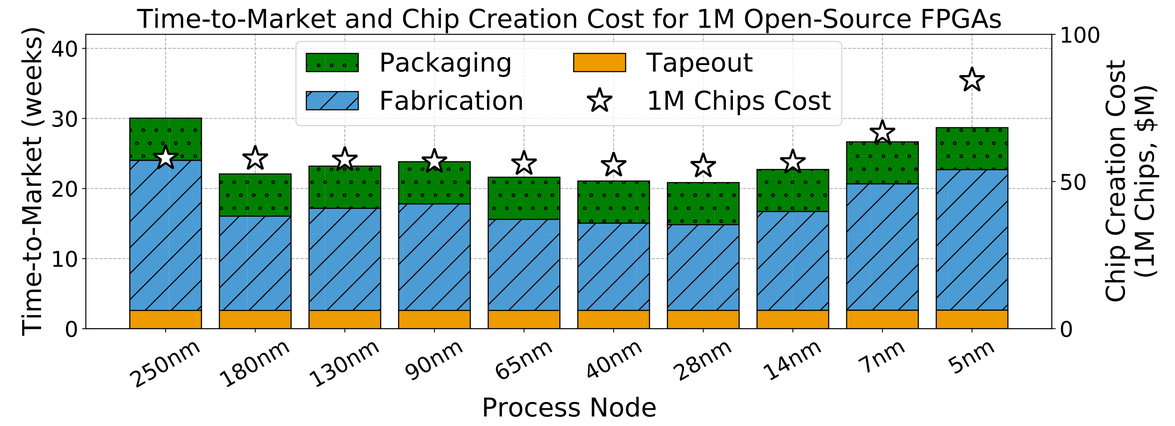


Evaluation

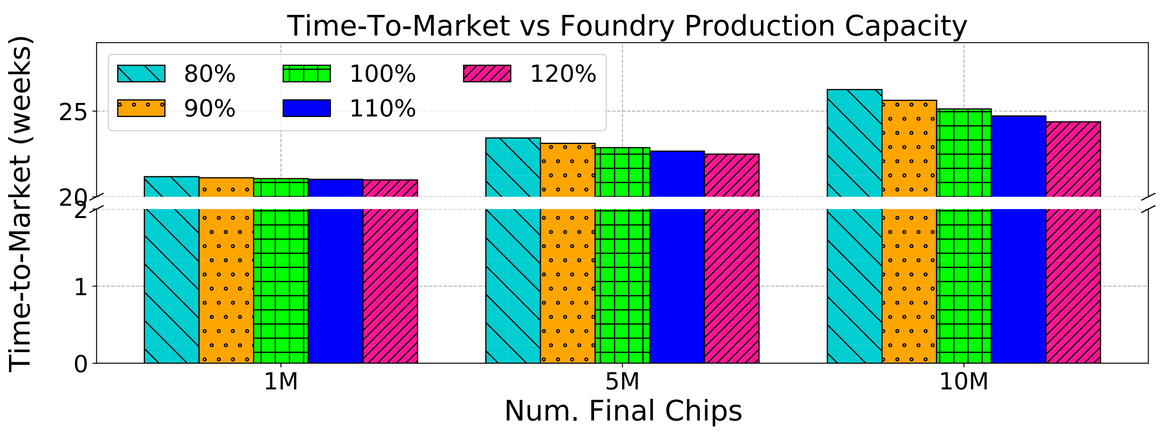
When producing at scale, proprietary designs become cheaper due to smaller die area



Time-to-market and chip creation costs are significantly influenced by process node choice



Increased production rates affect time-to-market only at massive chip quantities



Acknowledgment

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aning@princeton.edu
augustning.com
Princeton Parallel Group